Compatibility Advisory

Title	Compatibility Advisory for ESP32-C2 Chip Revision v2.0
Issue date	2025/03/03
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Serial Number	NA
Version	V1.0

Introduction

To provide more flash and SRAM space for application development on ESP32-C2 chips, we have upgraded the ESP32-C2 chip to revision v2.0. This latest chip revision, when paired with an upgraded ESP-IDF version, provides approximately 20 KB of additional SRAM and around 100 KB of extra flash space for development purposes (depending on actual application).

The increased memory availability is achieved by optimizing ROM code and relocating runtime-required code to ROM, without altering the physical sizes of SRAM and flash. For example, ESP32-C2 v2.0 implements partial mbedTLS cryptographic algorithm libraries in ROM to reduce flash usage. Note that ROM mbedTLS is disabled by default in ESP-IDF. Additionally, as ESP-IDF continues to evolve, some ROM functions may become deprecated, potentially resulting in less than 20 KB of usable SRAM and under 100 KB of flash savings (depending on actual application scenarios).

Given that the ROM functions for chip revision v2.0 have changed significantly, the binary compiled (hereinafter referred to as firmware) with older versions of ESP-IDF cannot run directly on chip revision v2.0. It is necessary to upgrade ESP-IDF to the required version or higher and recompile the firmware.

To support both v2.0 and legacy v1.x (v1.0–v1.2) chips at the same time, ESP-IDF can be configured to generate backward-compatible binaries. However, this configuration gives up the 20 KB SRAM and 100 KB flash optimizations from ROM enhancements.

Evaluation and Recommendations for Chip Revision Compatibility

In terms of hardware, ESP32-C2 chip revision v2.0 is compatible with earlier revisions.

The following description focuses on evaluating software compatibility. If you are currently using a pre-v2.0 chip and plan to adopt v2.0 chips, your existing ESP-IDF version may not support chip revision v2.0. You must upgrade ESP-IDF to the minimum required version. To upgrade ESP-IDF for supporting chip revision v2.0, the following scenarios are provided for quick reference.

Scenario	Need to Upgrade ESP-IDF to Specified Version?	"Minimum Supported ESP32-C2 Revision" in ESP-IDF menuconfig	Able to utilize the additional 20 KB SRAM and 100 KB flash?	Notes
Maintain firmware compatibility for both v2.0 and pre-v2.0 chips in the same project	Yes	Rev v1.0	No	If ESP-IDF is not upgraded, the compiled binary for pre-v2.0 chips cannot run on chip revision v2.0.
First-time adoption of v2.0 chips (no pre-v2.0 chips used previously)	Yes	Rev 2.0	Yes	Must use chip revision v2.0 and above in the future.
Use separate firmware for chip revision 2.0 and earlier revisions, aiming to utilize the additional SRAM and flash space with chip revision v2.0	Yes (recommend using the same ESP-IDF version to reduce maintenance costs)	Configure per scenarios above	Only v2.0 chips gain memory optimizations	Not recommended due to increased overhead for maintaining legacy firmware.

Required ESP-IDF Versions for Chip Revision v2.0

| Release branch	Recommended Version	Minimum Required Version
release/v5.4	v5.4 and above	v5.4
release/v5.3	v5.3.2 and above	v5.3.2

release/v5.2	v5.2.4 and above	v5.2.4
release/v5.1	v5.1.5 and above	v5.1.5
release/v5.0	v5.0.8 and above	v5.0.8

Note: Compatibility errors shown for versions v5.3.2 and v5.1.5 are false positives. To suppress these error messages, disable them by selecting the "ESP32C2_REV2_DEVELOPMENT" option in "menuconfig".

Required ESP-IDF Configuration for Using Chip Revision v2.0 and Above (to Obtain Additional Memory)

To utilize the additional resources of approximately 20 KB SRAM and 100 KB flash available in chip version v2.0, follow these steps:

1. Upgrade ESP-IDF to one of the required versions for chip revision v2.0 mentioned above.

2. Set "Minimum Supported ESP32-C2 Revision" in "menuconfig":
   When running the project configuration utility "menuconfig" of ESP-IDF, set "Minimum Supported ESP32-C2 Revision" (> Component config > Hardware Settings > Chip revision) as "Rev v2.0". The default value is "Rev v1.0".
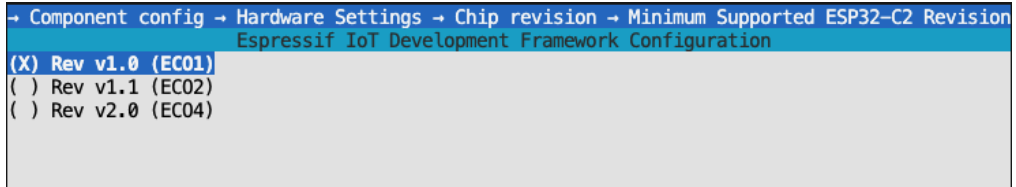
3. Compile and flash the software.

Required ESP-IDF Configuration for Firmware Compatibility with Both v2.0 and Pre-v2.0 chips

To compile firmware that supports both v2.0 and earlier chip revisions, follow these steps:

1. Upgrade ESP-IDF to one of the required versions for chip revision v2.0 mentioned above.

2. Set "Minimum Supported ESP32-C2 Revision" in "menuconfig":

When running the project configuration utility "menuconfig" of ESP-IDF, set "Minimum Supported ESP32-C2 Revision" (> Component config > Hardware Settings > Chip revision) as "Rev v1.0".

3. Compile and flash the software.

The option "Minimum Supported ESP32-C2 Revision" in "menuconfig" specifies the lowest expected compatible chip revision.

If "Minimum Supported ESP32-C2 Revision" in "menuconfig" is set to "Rev v2.0", the software will rely on the newly provided code in the ROM and remove the corresponding 20 KB functions that were originally located in the SRAM. Therefore, the binary file compiled with this option will not be able to run on chip revisions below v2.0.

If you need to support multiple chip revisions (e.g., v1.2 and v2.0), do not remove these functions. Instead, set "Minimum Supported ESP32-C2 Revision" to "Rev v1.0", ensuring compatibility with all mass-produced ESP32-C2 chip versions (including v1.0, v1.1, and v1.2). Then, recompile the firmware. The recompiled binary will be compatible with both v1.x and v2.0 chip revisions. However, the additional 20 KB of SRAM space will not be available.

When attempting to flash the compiled binary to a chip revision below v2.0, if the "Minimum Supported ESP32-C2 Revision" in "menuconfig" is set to "Rev v2.0", both the download tool (esptool) and the boot code (the second stage bootloader) will report errors. Below is the error message from the esptool tool:

A fatal error occurred: bootloader/bootloader.bin requires chip revision in range [v2.0 - v1.99] (this chip is revision v1.2). Use --force to flash anyway.

Identification of Chip Revisions

For how to identify chip revisions, please refer to ESP32-C2 Series SoC Errata. For explanations of software compatibility, please refer to Compatibility Between ESP-IDF Releases and Revisions of Espressif SoCs.

Contact

If you need technical assistance, please contact Espressif.